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# Update on GLAST Hodoscopic CsI Calorimeter

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# Hodoscopic Calorimeter Activities

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- Beamtest 97 - collect and analyze data from 8 layer hodoscopic calorimeter.
- Correlate Gismo simulations of hodoscopic calorimeter with Beamtest data - energy resolution, self-triggering modes, angular resolution (Jeff Skibo, Dan Suson, NRL; Jay Norris, Heather Muise, GSFC)
- Complete and submit Calorimeter prototype ASIC design (Satpal Singh, Prime Circuits, Inc./GSFC)
- Continue mechanical design of calorimeter packaging concept and alternatives (NRL, Hytec)
- Investigate effects determining CsI light output and impact on subsequent preamp gain.
  - Beamtest 97 (SLAC) position and energy resolution in EM showers
  - Hadronic Beam Test (NSCL, Michigan State) - position and energy resolution
  - Radiation Damage - light output vs irradiation dose
  - CsI block wrapping material and effects of compression cell loading
- Custom Pin Diode design

# CsI Calorimeter - 32 cm Tower

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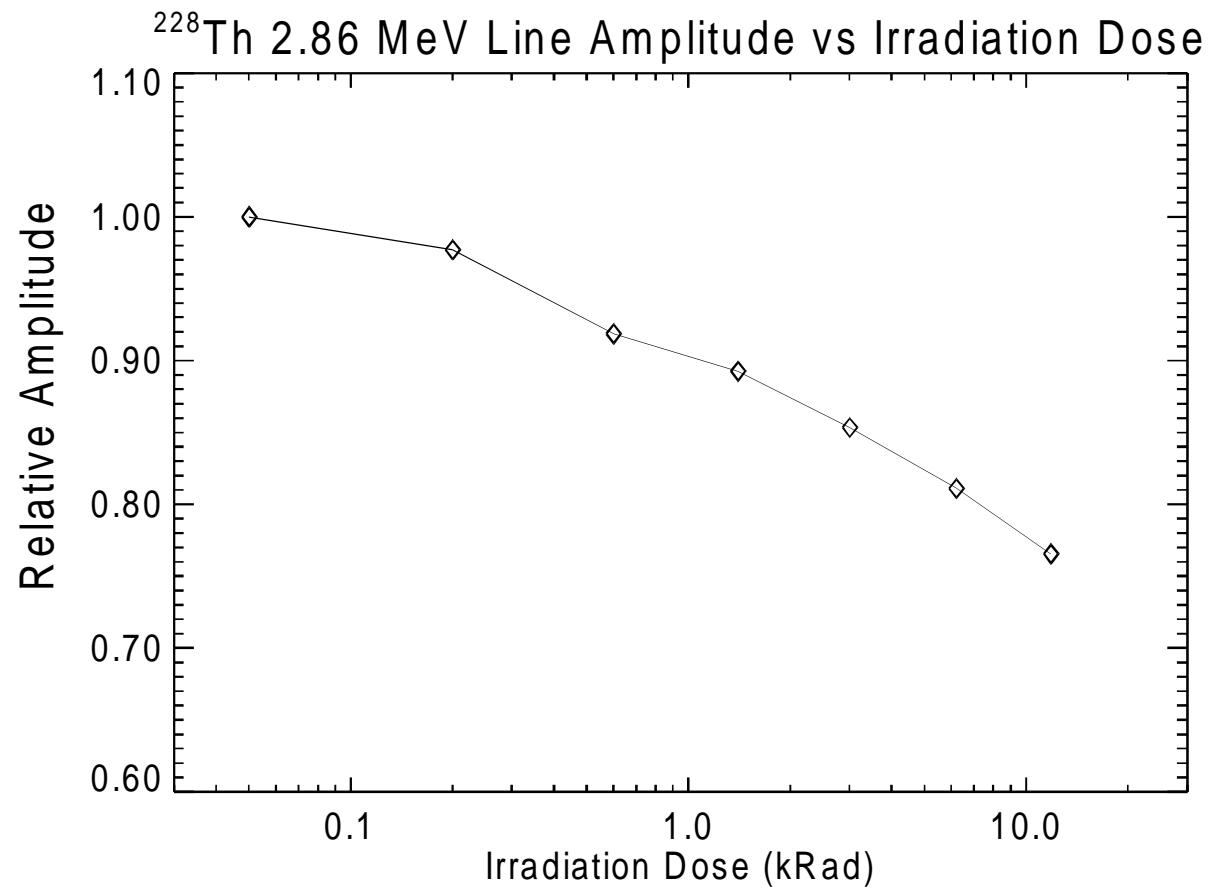
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- ❑ Calorimeter module is 8 layers of 10 CsI blocks.
  - ❑ Blocks are 3.1 x 2.3 x 31.0 cm in size.

# Light vs Radiation Dose

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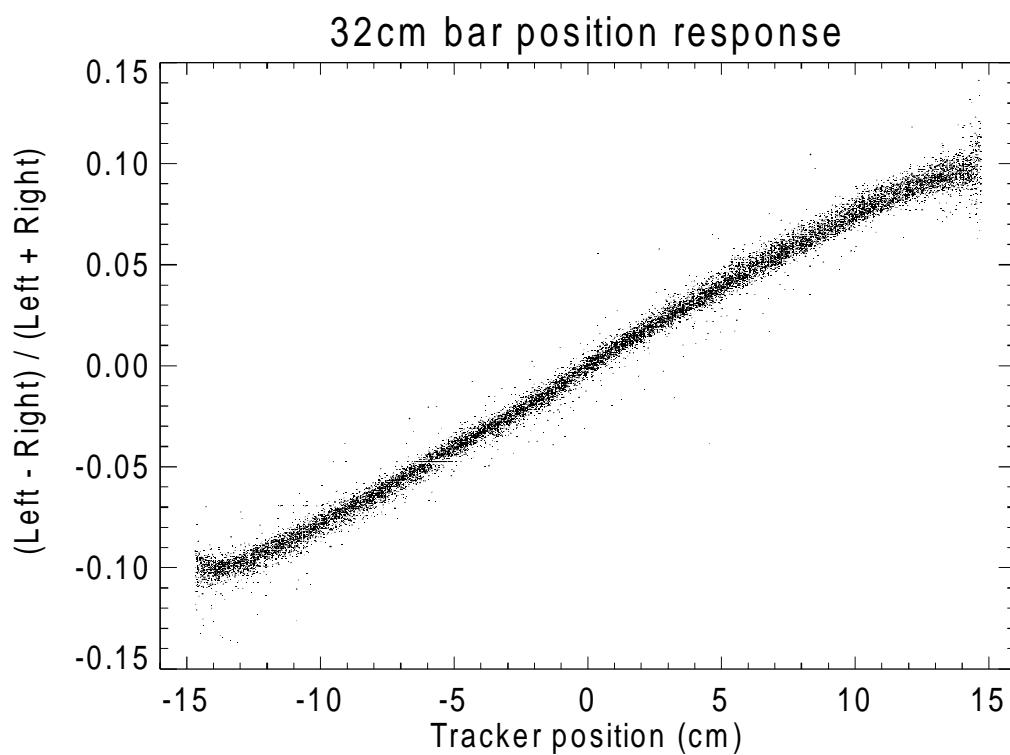
- Tests at NRL's  $^{60}\text{Co}$  Irradiation Facility
- Dose rate 50 - 200 Rad / hour
- Light loss caused by decrease in effective light attenuation length
- Varies depending on crystal growth process
- NRL results in agreement with Woody, et al. (BNL)



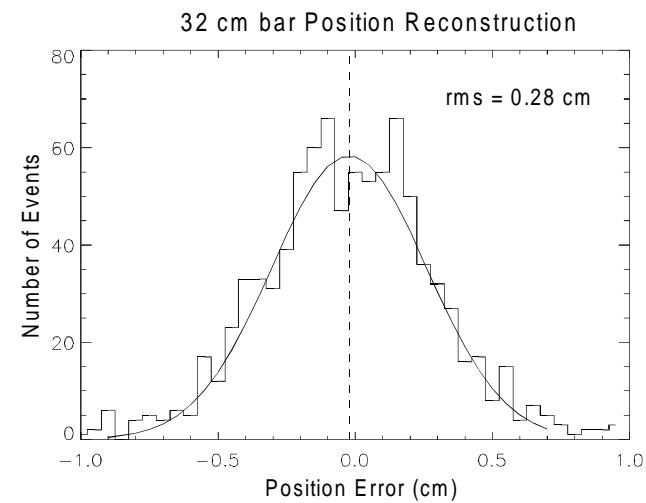
# Positioning with Light Amplitude Ratio

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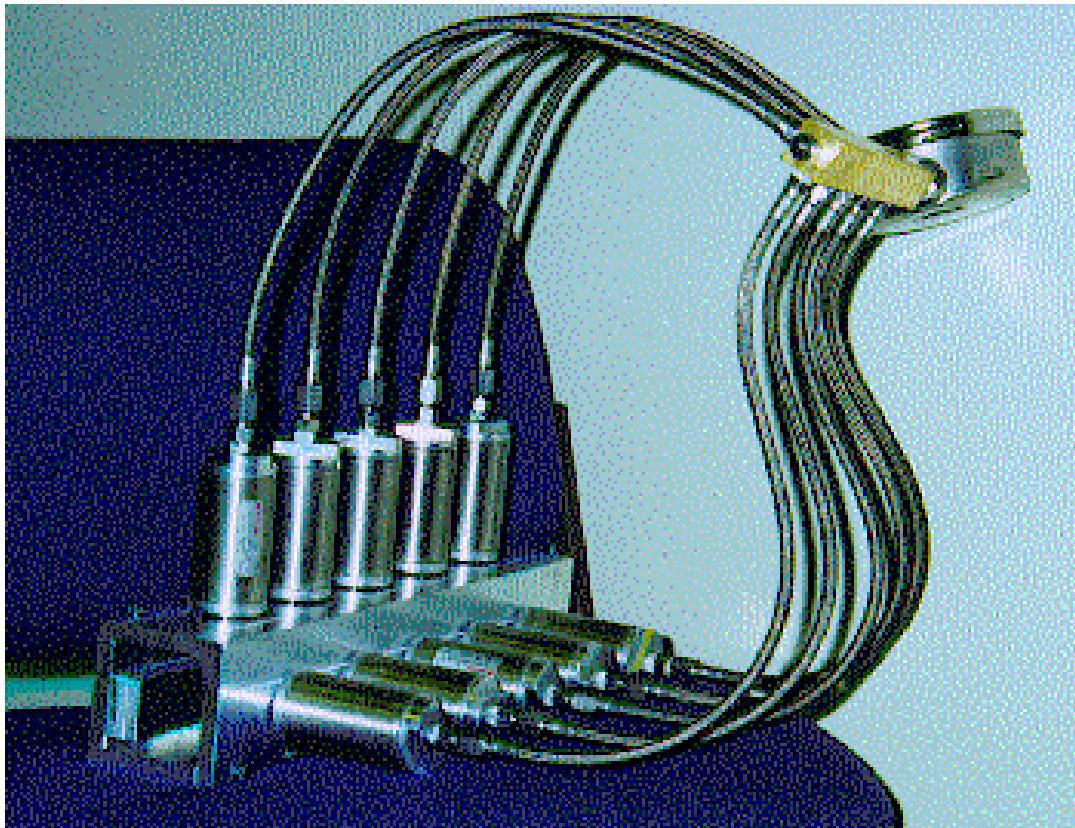


- SLAC  $e^-$  beam, 2 GeV
- $\Delta E \sim 130$  MeV



# Light Output with 10 G Loading

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- Crystal wrapping and surface treatments affect light output
- Compression of some wrapping (Teflon-like) for launch loads reduces light output
- Test with Tyvek and Tetratek
- Use compression chamber to load individual crystals

# Photo Electron Yield Estimate

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**SLAC and MSU tests @ 21 deg C, 19 cm logs:**

PIN collects 12,000 - 15,000  $e^-$  / MeV

## **Reductions:**

- Operation at 0 deg C, reduce by factor ~ 0.9 (Blucher et al., CLEO)
- Radiation effects (10 kRad), reduce by factor ~ 0.75
- Channel gain variation in ASIC (+/- 10%), reduce by factor ~ 0.9
- Light output variation in crystals and wrapping (+/- 20%), reduce by factor ~ 0.8

## **Result:**

6,000 - 8,000  $e^-$  / MeV (prototype ASIC designed at 10,000  $e^-$  / MeV)

**Other Issues:** Custom PIN diode active area